(9) CLAIMS

1. An integrated circuit structure including chip-scale packaging, the structure comprising:

a first die, having at least one first input-output bump, associated redistribution beam and associated die pad;

a second die, having at least one second input-output bump, associated distribution beam and associated die pad; and

an electrical interconnect between the first die and the second die wherein the electrical interconnect uses at least one same metallization layer forming each said redistribution beam.

2. The structure as set forth in claim 1 wherein said at least one same metallization layer further comprises a top metal layer of at least one of said die.

3. The structure as set forth in claim 1 further comprising:

a plurality of more than two dice and a plurality of electrical interconnects between said plurality of more than two dice using the at least one same metallization layer.

4. The structure as set forth in claim 3 in a wafer-scale integrated circuit device.

5. The structure as set forth in claim 1 wherein said structure is formed on a wafer having scribe line region between said first die and said second die, a polyimide-like bridge across said region and superjacent an active component surface of said first die and said second die and subjacent said at least one same metallization layer.

6. An integrated circuit chip set comprising:

a plurality of discrete integrated circuit devices, each of said devices including discrete circuit elements and associated input-output pads, wherein each of said devices includes chip-scale bump input-output terminals connected by conductive material layer beams to the electrical pads; and

electrical traces connecting said discrete integrated circuit devices wherein said electrical traces are concomitant with the conductive material layer forming the beams.

7. The integrated circuit chip set as set forth in claim 6 in a wafer-scale integrated circuit device.

8. The integrated circuit chip set as set forth in claim 6 further comprising:

a dielectric material layer subjacent said electrical traces.

9. The integrated circuit chip set as set forth in claim 6 wherein said plurality of discrete integrated circuit devices are connected in parallel via said electrical traces.

10. The integrated circuit chip set as set forth in claim 6 wherein said plurality of discrete integrated circuit devices are connected in via said electrical traces such that said traces are formed concurrently with a top metal layer of said discrete integrated circuit devices.

11. An integrated circuit die chip set, each die having bipolar components, MOSFET components, or both, said components sharing a common top metal layer and input-output pads respectively, each die further including bump out contacts with metal beams for connecting bumps thereof to said pads, respectively, the chip set further comprising:

said metal beams are formed integrally with said common top metal layer; and said top metal layer further forms a die-to-die electrical connection bridge.

12. The chip set as set forth in claim 11 further comprising:
a dielectric layer subjacent said bridge.

13. The chip set as set forth in claim 12 wherein said dielectric layer comprises:
a layer of benzocyclobutene.